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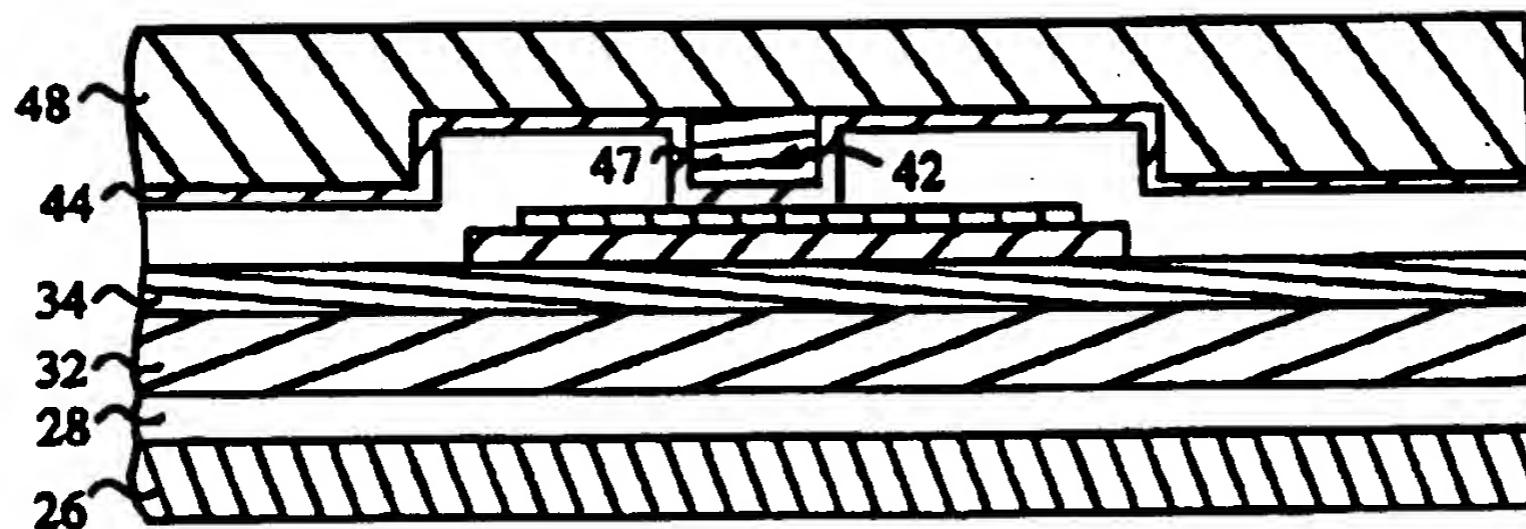
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(54) Title: AN ANTI-FUSE STRUCTURE AND METHOD FOR MAKING SAME



(57) Abstract

An anti-fuse structure formed in accordance with the present invention includes a conductive layer base. A layer of anti-fuse material (38) overlies the conductive base layer (36). On top of the anti-fuse layer (38) is an insulating layer (40), in which a via hole (42) is formed to the anti-fuse layer (38). The lateral dimension of the via hole (42) is less than about 0.8 microns. Provided in the via hole (42) is a conductive non-Al plug (47) filling the via (42) as well as a conductive barrier material (44) such as TiN or TiW to contact the anti-fuse material (38) and overlie the insulating layer (40). Tungsten is effectively used as the non-Al plug (47). A top layer of Al (48) is also possible included in the structure over the conductive barrier material (44). The structure is then programmable by application of a programming voltage and readable by application of a sensing voltage, which is lower than the programming voltage.

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AN ANTI-FUSE STRUCTURE AND METHOD FOR MAKING SAMEDescriptionTechnical Field

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This invention relates generally to integrated circuits and, more specifically, to anti-fuse structures in integrated circuits.

Background Art

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Programmable integrated circuits include such devices as field-programmable gate arrays and programmable read-only memories (PROMS). Such devices may include elements such as fuses or anti-fuses to enable them to be programmed.

Field programmable gate arrays include a large number of logic elements, such as AND gates and OR gates, which can be selectively coupled together by devices like fuses or anti-fuses to perform user-designed functions. The several types of PROMS, including standard, write-once PROMS, erasable programmable read-only memories (EPROMS), electrically erasable programmable read-only memories (EEPROMS), etc., usually comprise an array of memory cells arranged in rows and columns which can be programmed to store user data. An unprogrammed anti-fuse gate array or PROM is programmed by causing selected anti-fuses to become conductive.

Anti-fuses include a material which initially has a high resistance but which can be converted into a low resistance material by the application of a programming voltage. For example, amorphous silicon (A-Si), which has an intrinsic resistivity of approximately 1 megohm-cm, can be fashioned into 1 micron wide vias having a resistance of approximately 1-2 gigohms. These vias can then be transformed into a low resistance state by the application of a voltage in the range of 10-12 volts d.c. to form vias having a resistance less than 200 ohms. These low resistance vias can couple together logic elements of a field programmable gate array so that the gate array will perform user-defined functions or connect large functional blocks, or can serve as memory cells of a PROM.

an anti-fuse device is typically formed on a semiconductor wafer by depositing a bottom electrode layer, such as titanium-tungsten (TiW), depositing an oxide layer over the electrode layer, forming a via through the oxide layer to the electrode layer, and depositing 5 A-Si into the via. A second layer of TiW can be deposited over the A-Si with an aluminum (Al) layer deposited over the TiW layer.

Problems arise in the above-described structure by "cusing" or thinning of the A-Si at the corners of the via that can lead to leakage and programming problems. Further, cusps formed in the A-Si layer can lead to poor step coverage of the TiW layer over the A-Si. This 10 can cause an inadequate TiW barrier to be formed separating the top Al layer from the A-Si, which can compromise the reliability of the anti-fuse, because Al is known to degrade or "poison" an anti-fuse structure by diffusing into the A-Si layer.

A prior art solution to this problem provides oxide spacers over the cusps of the A-Si. Such a structure is described in U.S. Patent 5,120,679 issued to Boardman et al., the 15 disclosure of which is incorporated herein by reference. This spacer better protects the corners of the via where the cusping or thinning of the A-Si is problematic. The spacer also improves the topography for the subsequent TiW barrier layer deposition. The use of dielectric spacers reduces leakage current and enhances reliability. However, the use of spacers may increase production time and cost. Further, the use of spacers results in 20 reduced scalability of the structure below 1.0 micron (μm).

Alternatively, another anti-fuse structure is used for technology scaled to 0.8 μm , as the cross-sectional view of the anti-fuse structure in Figure 1 illustrates. Overlying a silicon wafer substrate 8 on which a base oxide layer 9 has been formed are a first metal layer 10 (typically Al) and an inter-metal oxide (IMO) layer 12. A layer 14 of TiW is deposited and 25 patterned to form a conductive "strap". Following formation of layer 14, a layer of A-Si 16 is deposited and then patterned to remain only in the desired locations overlying the TiW patterned layer 14. Thus, the A-Si is not deposited in the via as in the prior anti-fuse structures, but rather, forms a separate, planar layer. An oxide layer 18 is then deposited, followed by the etching of a via 20 through the oxide layer 18 to the A-Si layer 16. A 30 barrier layer 22 of TiW is then preferably deposited over the oxide and into the via 20 to contact the A-Si layer 16. Subsequently, metal layer 24, preferably Al, is then deposited over the TiW layer, which prevents the Al layer 24 from poisoning the A-Si layer 16.

While the above-described structure is usable with 0.8 μm anti-fuse technology, the integrity of the anti-fuse is dependent on the integrity of the TiW barrier layer 22. This

barrier layer has a problem of cusping or thinning at the corners 21 of the via 20. This cusping makes the corners more permeable to the migration of Al atoms from layer 24, which can lead to Al layer 24 diffusing into the A-Si layer 16, thereby "poisoning" the A-Si 5 layer 16 at that point. By "poisoning" it is meant that the conductive aluminum atoms in the A-Si layer change the conductivity of the layer such that it cannot be properly programmed or read. The problem increases as the via is scaled to widths below 0.8 μm .

What is needed is an anti-fuse structure that retains the simplicity of the planar A-Si approach as illustrated in Fig. 1, but which does not have the problems associated with this 10 approach, especially as the via width is scaled below 0.8 μm .

Disclosure of the Invention

5 In accordance with the present invention, an anti-fuse structure and method for forming an anti-fuse structure are described. In general, the anti-fuse structure uses a planar anti-fuse layer and is scalable to sub-micron size. Further, the problem of Al migration into the anti-fuse layer is overcome by the use of a non-Al conductor as a plug within the via hole.

10 A method for making an anti-fuse structure begins with the formation of a conductive base layer. An anti-fuse layer is then formed over the conductive base layer. Following this, an insulating layer is formed over the anti-fuse layer. A via hole is then etched through the insulating layer to the anti-fuse layer with the lateral dimension of the via being no more than approximately 0.8 microns. A conductive barrier material is then used to form a layer over the insulating layer and in the via hole to contact the anti-fuse layer.
15 The conductive barrier material preferably consists essentially of TiW or TiN. A W layer is deposited after the conductive barrier material layer is formed. This W layer is preferably formed as a blanket layer, which is then etched-back to form a W plug in the via hole. An Al layer is preferably formed over the conductive barrier material and the W plug to act as the top conductive layer. The completed anti-fuse structure is then programmable by
20 applying a programming voltage between the conductive base layer and the conductive barrier material, and is readable by application of a lower, sensing voltage between the layers, as is conventional in the art.

25 An anti-fuse structure in accordance with the present invention includes a conductive layer base. A layer of anti-fuse material overlies the conductive base layer. On top of the anti-fuse layer is an insulating layer, in which a via hole is formed to the anti-fuse layer. The lateral dimension of the via hole is preferably less than about 0.8 microns. Provided in the via hole to contact the anti-fuse material and over the insulating layer is a conductive barrier material preferably including either TiN or TiW. The structure also includes a W plug. This plug is formed by blanket deposition over the conductive barrier material, which
30 is subsequently etched-back by well known processes. A top layer of Al is further included in the structure over the conductive barrier material. The structure is then programmable by application of a programming voltage and readable by application of a sensing voltage, which is lower than the programming voltage.

-5-

An advantage of the anti-fuse formed by the present invention is that there is no aluminum in the via hole to potentially poison the amorphous silicon. Further, the material and process used to form the non-aluminum vias are standard, so that the process and 5 structure of the present invention are quite compatible with and easily incorporated into conventional semiconductor manufacturing processes.

These and other advantages of the present invention will become apparent upon reading the following detailed descriptions and studying the various figures of the drawings.

Brief Description of the Drawings

Fig. 1 is a cross-sectional view of an anti-fuse structure of the prior art;

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Figures 2-5 illustrate a step-by-step cross-sectional views of an anti-fuse structure formed in accordance with the present invention;

10 Figures 6-7 illustrate cross-sectional views of alternate anti-fuse structures in accordance with the present invention;

Figure 8 is a flow diagram illustrating an overall process for forming an anti-fuse structure in the present invention; and

15 Figures 9a-9c are flow diagrams illustrating alternative processes for performing step 56 in the process shown in Fig. 8.

Best Modes for Carrying out the Invention

Figure 1 was discussed in terms of the prior art. Figures 2-7 present step-by-step cross-sectional views of the formation of an anti-fuse structure by the methods of the present invention. In Figure 2, processed substrate 30 includes a semiconductor wafer 26 (such as a silicon wafer), a base oxide layer 28 formed over the semiconductor wafer 26, a first metal layer 32 formed over the oxide layer 28, and an inter-metal oxide (IMO) layer 34 formed over the first metal layer 32. As described to this point, the structure is substantially standard to the industry.

A strap layer 36 of TiW is formed over these layers. The TiW of strap 36 is preferably sputter deposited to a thickness between about 1000 and 10,000 angstroms (\AA), with 2200 \AA being a preferable thickness. The TiW layer 36 is then patterned by standard photolithographic and etch techniques to form the strap 36.

As used herein, the term "patterned" refers to photolithographic etch techniques, whereby a resist material is applied to the upper surface of the layer being patterned, is exposed to a pattern of radiant energy, and is then developed to form a mask. An etching process is undertaken to etch away the surface of the layer through the mask. At the end of the photolithography process, the mask is typically removed.

A layer 38 of anti-fuse material such as A-Si is then deposited and patterned to remain only over the strap 36. Deposition is preferably performed by standard plasma enhanced chemical vapor deposition (PECVD) process. A range for the thickness of this layer 38 is between about 500-5000 \AA , with 1200 \AA being a preferred thickness for 0.8 μm technologies.

Figure 3 illustrates the structure of Fig. 2 with the addition of an insulating layer 40. Silicon dioxide is a suitable material to use for this insulating layer, and PECVD is the preferable deposition method. An appropriate thickness for layer 40 is in the range of approximately 1000-10,000 \AA , with 3000 \AA having been found to work well. A via 42 is formed by patterning layer 40 by standard photolithographic and etch techniques. The lateral dimension "D" or width of the via is scalable to a desired dimension, but is preferably below about 0.8 μm , more preferably below about 0.6 μm . Of course, the structure can also be used with vias having greater than 0.8 μm lateral dimensions, but is particularly suitable for sub-micron applications.

In a first preferred embodiment of the present invention, as seen in Figure 4, a conformal barrier layer 44 of a non-aluminum conductor is deposited over the insulating layer 40 and into the via 42. Suitable non-aluminum conductors include, for example, TiW and TiN (titanium-nitride). The thickness of this layer is preferably between about 500-3000 Å, with 1000 Å having been found to work well. A suitable deposition process for a TiN layer is chemical vapor deposition (CVD) or sputter deposition, while sputter deposition techniques are suitable for TiW. A plug layer 46 is then deposited as a blanket layer over the barrier layer 44. Tungsten is preferably used as the plug layer 46, but W is not able to adhere well to the insulating oxide layer 40 so that the TiW or TiN also acts as an adhesion layer for the W plug deposition. The plug layer 46 is deposited to a thickness preferably approximately 0.8 times the lateral dimension "D" of the via 42, where, in this example D is preferably about 0.8 μm.

Figure 5 illustrates the structure of Fig. 4 following etch-back of the plug layer 46. This forms a W plug 47 in the via hole 42. By way of example, etch-back of the plug layer is performed by plasma etch techniques well known to those skilled in the art. A layer 48 of aluminum is then deposited over the plug 47. With the plug 47, the conductive layer 48 is kept well away from the A-Si layer 38, and thus the possibility of degradation of the anti-fuse structure due to diffusion of the aluminum layer 48 into the anti-fuse layer 38 is all but eliminated.

The via hole 42 has a depth (after the barrier layer 44 is provided) which extends from the top surface of the barrier layer 44 that is within the via hole 42 to the rim of the via hole 42 that has been raised by the thickness of the barrier layer 44. As such, the depth of the via hole 42 is about the same depth of the via hole 42 before the barrier layer 44 was deposited. Preferably, the plug 47 has a height equal to at least one-half (1/2) of the depth of the via hole 42. This ensures that any aluminum is kept well away from the anti-fuse layer and further ensures that the crucial corners of the via hole 42 are filled with plug material.

Alternatives to the structure of Figure 5 that maintain the separation of the aluminum layer from the anti-fuse layer are illustrated in Figures 6 and 7. As shown in Fig. 6, the plug layer 46 is not etched-back from the via opening 42. Rather, the entire layer 46 remains over the barrier layer 44 and is also patterned as an interconnect. For low resistance interconnects, the conductive layer 48 is deposited over this blanket layer 46, and the two layers are patterned together. This, again, separates the aluminum layer 48 from the A-Si layer 38.

Another alternative, as shown in Fig. 7, eliminates the layer 46. The barrier layer 44 when formed with TiN is capable of serving as a non-Al plug. TiN is suitable since it is deposited by CVD and is therefore capable of filling the via 42. TiW, on the other hand, is deposited by sputter deposition and thus, would be unsuitable for filling the via 42. The 5 TiN restricts the diffusion of the conductive layer 48 into the anti-fuse layer 38, while also acting as a suitable conductor during programming of the anti-fuse structure. In this embodiment, a suitable thickness of the TiN is approximately 0.8 times the lateral dimension "D" of the via 42.

It is therefore a key element of the present invention to use a non-Al conductive plug 10 in the via hole over an A-Si anti-fuse layer. By "non-Al" plug, it is meant that the great majority of the atoms of the material within the via are not free Al atoms that can react with the A-Si. For example, any Al atoms in the TiW or TiN should be less than one part per million (ppm). Of course, it is impossible to provide absolutely pure materials to form 15 plugs within vias, but the essence of the present invention is to minimize, to the extent practical, the number of Al atoms within the via in proximity to the A-Si layer, thereby forming a substantially non-Al plug within the via.

It should also be noted that the term "non-Al plug" covers a variety of structures. In 20 one embodiment, the "non-Al plug" is a conformal TiW barrier layer with a "W plug" formed inside. In another embodiment, the "non-Al plug" is a conformal TiN barrier layer with a "W plug" formed inside. In a third embodiment, the "non-Al plug" is made from TiN. Therefore, the term "non-Al plug" will mean one or more conductive materials deposited within a via, which singly or together substantially fill the via.

The flow diagram of Figure 8 illustrates a process 49 in accordance with the present 25 invention. As shown, the process 49 begins with step 50 and the deposition and patterning of a strap layer over an initial substrate. The substrate is preferably an IMO layer overlying a metal layer such as Al, which is formed on a prepared silicon wafer or the like, as shown and described with reference to Fig. 2. TiW is suitable for use as the strap layer. Standard photolithographic techniques are preferably utilized to pattern the strap layer. At this stage 30 of the process, the structure corresponds to layers 26-36 of Figure 2.

Following the deposition and patterning of the strap layer, a layer of anti-fuse material such as A-Si layer 38 is deposited, such as by PECVD, and patterned in step 52. A preferable range for the thickness of this layer is between about 500-5000 Å, with 1200 Å 35

being a suitable thickness for 0.8 μm technologies. Following the patterning step, the structure appears as illustrated in Fig. 2.

After patterning of the anti-fuse layer 38 is completed, an insulating layer 40 is
5 deposited in step 54. Silicon dioxide is appropriate for this insulating layer. A via 42 is then etched through the insulating layer in the areas where the anti-fuse material is located. The via is preferably established by plasma etching through the insulating layer by techniques well known to those skilled in the art. The lateral dimension of this via is preferably no greater than about 0.8 μm , with less than 0.8 μm (e.g., 0.6 μm) being more
10 preferable. At this point of the process, the structure appears as illustrated in Figure 3.

The process 49 continues with step 56 and the deposition of a non-Al conductor barrier layer 44 over the insulating layer and into the via. It is at this point in the process that alternative procedures are possible, as illustrated in the flow diagrams of Figures 9a-9c. As shown in Fig. 9a, in one embodiment, a process 56a involves three steps. First, in step
15 58, a barrier layer of a non-Al conductor is conformally deposited over the insulating layer and into the via establishing contact with the anti-fuse material. TiN, TiW, and other like materials are usable for this step. The thickness of this layer is in the range of about 500-3000 Å, with 1000 Å having been found to work well. Next, a plug layer, suitably comprised of W, is deposited over the barrier layer in step 60. A suitable thickness of the
20 plug layer is approximately 0.8 times the lateral dimension D of the via 42. Then, in step 62, the plug layer is etched-back to form a plug in the via hole. The structure resulting from this process is shown with reference to Figure 5.

Alternatively, the flow diagram of Figure 9b illustrates another embodiment, process 56b. This process is similar to that shown in Figure 9a, except that step 60, the etch-back
25 step, is not performed in this method. Rather, the plug layer remains over the entire barrier layer and in the via. This arrangement is illustrated and described with reference to Figure 6.

A third alternative for process 56c is illustrated in Figure 9c. This embodiment comprises only a single step 64 of depositing a barrier/plug layer. For this embodiment, the
30 barrier layer preferably comprises TiN since the layer needs to be able to form a plug in the via hole, and TiN is suitably capable of being deposited as a plug by CVD. TiN, besides being well-suited for plug formation by CVD deposition, also adheres well to silicon dioxide (SiO_2) unlike W. TiW would not be a material as satisfactory for use as a plug due to the required use of sputter deposition for its application, which could cause cusping,

voids, and other defects. An appropriate thickness of the TiN for this embodiment is approximately 0.8 times the lateral dimension D of the via. The structure occurring with this embodiment is described in conjunction with Figure 7.

5 The process then continues with the sequence illustrated in Figure 8. Following step 56, (i.e., one of the processes 56a, 56b, or 56c) the next step 66 is the deposition of a conductive layer, e.g., Al, over the non-Al conductor layer. Alternatively, as the dashed arrow 66' indicates, since the barrier layer formed in step 56 is a conductive layer, the Al layer can be eliminated in some instances, so that the process could end following step 56.

10 In either case, the anti-fuse structure maintains a lower conductive layer, an anti-fuse layer, and a top conductive layer with a via plug of a non-Al material connecting the top conductive layer with the bottom conductive layer through the anti-fuse layer. Accordingly, with this structure, anti-fuse programming is accomplished by applying a programming voltage of approximately 10 volts (V) between the conductive layers, and subsequent reading of the

15 anti-fuse structure is accomplished by applying an appropriate sensing voltage, as is well known to those skilled in the art.

Although only a few embodiments of the present invention have been described in detail, it should be understood that the present invention may be embodied in many other specific forms without departing from the spirit or scope of the invention. Particularly, the

20 invention has been described in the context of a strap layer comprised of TiW. Alternatively, the TiW could be replaced with W. Further, the non-Al conductive barrier layer could be formed using chromium in addition to or instead of the TiN and TiW described. Further, the range of thicknesses for the A-Si layer has been selected so that the layer is not too thin which could lead to leaking or too thick which would require a high programming voltage. Of course, in alternate applications having higher programming voltage capabilities, the upper limit on the range of thicknesses could be increased.

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It is therefore intended that the following appended claims be interpreted as including all such alterations, permutations, and equivalents as fall within the true spirit and scope of the present invention.

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What is claimed is:

Claims

1. A method for making an anti-fuse structure comprising the steps of:
 - 1 forming a conductive base layer;
 - 2 forming a layer of anti-fuse material over said conductive base layer;
 - 3 forming an insulating layer over said anti-fuse layer;
 - 4 forming a via hole having a lateral dimension no greater than about 0.8 microns through said insulating layer to said anti-fuse layer; and
 - 5 providing a conductive non-Al plug to fill said via hole, said plug including a barrier material selected from the group consisting essentially of TiW, TiN, and chromium within said via hole and in contact with said anti-fuse layer;
 - 6 such that said anti-fuse structure may be programmed by providing a programming voltage between said conductive base layer and said conductive barrier material, and may be read by providing a sensing voltage, which is lower than said programming voltage,
2. A method as recited in claim 1 wherein said lateral dimension of said via hole is no greater than about 0.6 microns.
3. A method as recited in claim 1 wherein said conductive barrier material is conformally deposited within said via, and wherein said non-Al plug further includes a W plug within said via hole and in contact with said conductive barrier material.
4. A method as recited in claim 3 further comprising the step of providing a conductive line comprising aluminum over said conductive barrier material and in contact with said W plug.

5. A method as recited in claim 3 wherein said W plug is provided by a deposition process which provides a blanket of tungsten over said conductive barrier material and within said via hole.

5

6. A method as recited in claim 5 further comprising the step of etching-back said blanket of tungsten to substantially remove said blanket of tungsten outside of said via hole.

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7. A method as recited in claim 6 further comprising the step of providing a conductive line comprising aluminum over said insulating layer and in contact with said W plug.

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8. A method as recited in claim 1 wherein said conductive barrier material comprises TiN, which substantially completely fills said via hole as said non-Al plug.

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9. A method as recited in claim 1 wherein said conductive base layer is provided with a thickness in the range of about 1000-10,000 Å.

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10. A method as recited in claim 9 wherein said conductive base layer is provided with a thickness of about 2200 Å.

11. A method as recited in claim 1 wherein said anti-fuse material is formed with a thickness in the range of about 500-5,000 Å.

12. A method as recited in claim 11 wherein said anti-fuse material is formed with a thickness of about 1200 Å.

13. A method as recited in claim 1 wherein said insulating layer is formed with a thickness in the range of about 1000-10,000 Å.

5 14. A method as recited in claim 13 wherein said insulating layer is formed with a thickness of about 3000 Å.

10 15. A method as recited in claim 1 wherein said conductive barrier material is provided with a thickness in the range of about 500-3000 Å.

16. A method as recited in claim 15 wherein said conductive barrier material is provided with a thickness of about 1000 Å.

17. A method as recited in claim 3 wherein said via hole has a depth, and wherein
15 said W plug is provided with a height of at least 1/2 of said depth of said via hole.

18. A method as recited in claim 5 wherein said blanket layer of tungsten is provided with a thickness of about 0.8 times the lateral dimension of the via hole.

20 19. A method as recited in claim 8 wherein said barrier material has a thickness of about 0.8 times the lateral dimension of the via hole.

20. An anti-fuse structure comprising:

a conductive base layer;

25 a layer of anti-fuse material formed over said conductive base layer;

an insulating layer formed over said anti-fuse layer, said insulating layer being provided with a via hole to said anti-fuse layer, and said via hole having a lateral dimension no greater than about 0.8 microns; and

5 a conductive non-Al plug filling said via hole including a barrier material consisting essentially of the group consisting essentially of TiW, TiN, and chromium, provided within said via hole and in contact with said anti-fuse layer;

such that said anti-fuse structure may be programmed by providing a programming voltage between said conductive base layer and said conductive barrier material, and may be
10 read by providing a sensing voltage, which is lower than said programming voltage, between said conductive base layer and said conductive barrier material.

21. An anti-fuse structure as recited in claim 20 wherein said lateral dimension of said via hole is no greater than about 0.6 microns.

15

22. An anti-fuse structure as recited in claim 20 wherein said conductive barrier material is conformal within said via, and wherein said non-Al plug further comprises a W plug within said via hole and in contact with said conductive barrier material.

20 23. An anti-fuse structure as recited in claim 22 further comprising a conductive line comprising aluminum over said conductive barrier material and in contact with said W plug.

24. An anti-fuse structure as recited in claim 22 wherein said W plug is a part of
25 a blanket layer of tungsten over said conductive barrier material and within said via hole.

25. An anti-fuse structure as recited in claim 24 wherein said tungsten blanket layer is patterned to provide a tungsten interconnect contacting said plug.

26. An anti-fuse structure as recited in claim 22 further including a conductive line comprising aluminum over said insulating layer and in contact with said W plug.

5 27. An anti-fuse structure as recited in claim 20 wherein said barrier material comprises TiN which substantially completely fills said via hole as said non-Al plug.

28. An anti-fuse structure as recited in claim 20 wherein said conductive base layer has a thickness in the range of about 1000-10,000 Å.

10

29. An anti-fuse structure as recited in claim 28 wherein said conductive base layer has a thickness of about 2200 Å.

15 30. An anti-fuse structure as recited in claim 20 wherein said anti-fuse material has a thickness in the range of about 500-5,000 Å.

31. An anti-fuse structure as recited in claim 30 wherein said anti-fuse material has a thickness of about 1200 Å.

20 32. An anti-fuse structure as recited in claim 20 wherein said insulating layer has a thickness in the range of about 1000-10,000 Å.

33. An anti-fuse structure as recited in claim 32 wherein said insulating layer has a thickness of about 3000 Å.

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34. An anti-fuse structure as recited in claim 20 wherein said conductive barrier material has a thickness in the range of about 500-3000 Å.

5 35. An anti-fuse structure as recited in claim 34 wherein said conductive barrier material has a thickness of about 1000 Å.

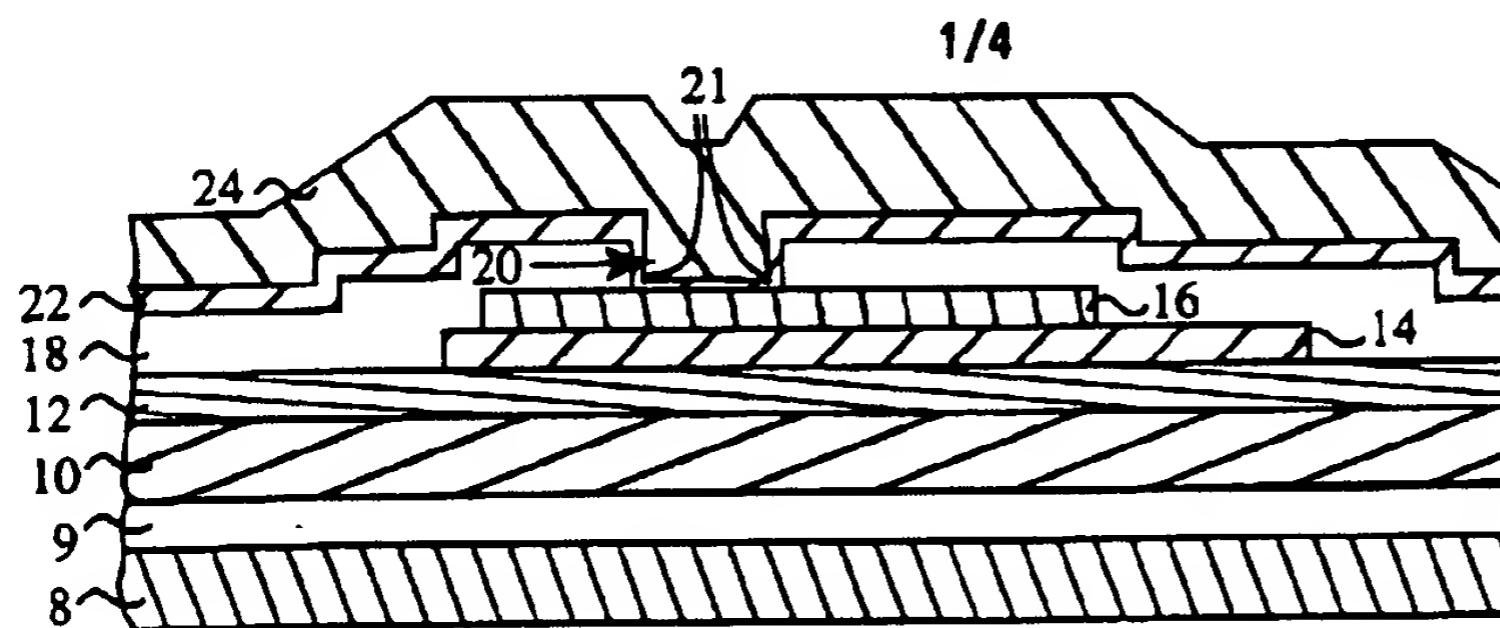
36. An anti-fuse structure as recited in claim 22 wherein said via hole has a depth, and wherein said W plug has a height of at least 1/2 of said depth of said via hole.

10

37. An anti-fuse structure as recited in claim 24 wherein said blanket layer of tungsten has a thickness of about 0.8 times the lateral dimension of the via hole.

15 38. An anti-fuse structure as recited in claim 27 wherein said barrier material has a thickness of about 0.8 times the lateral dimension of the via hole.

39. An anti-fuse structure as recited in claim 25 further comprising an aluminum interconnect provided over said tungsten interconnect.



*FIG. 1
(Prior Art)*

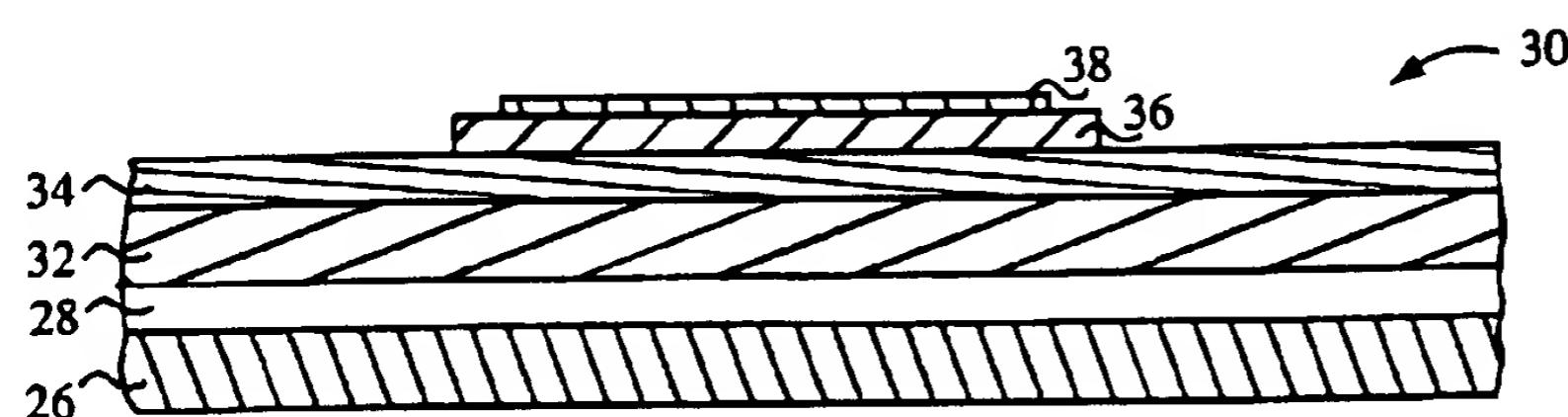


FIG. 2

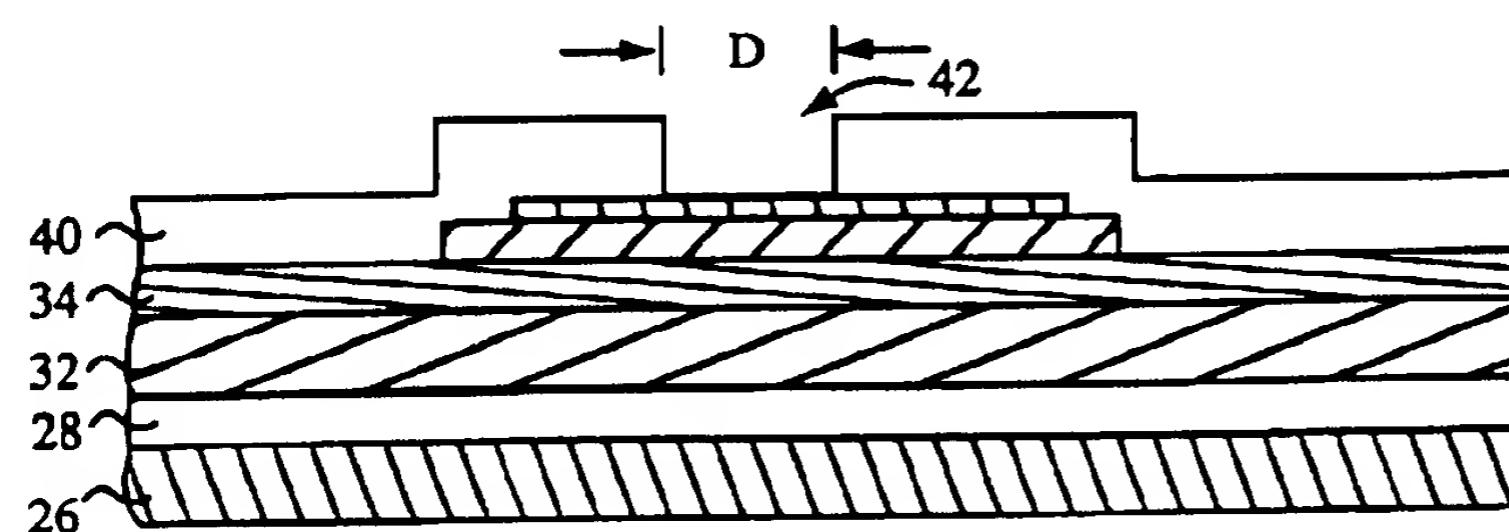


FIG. 3

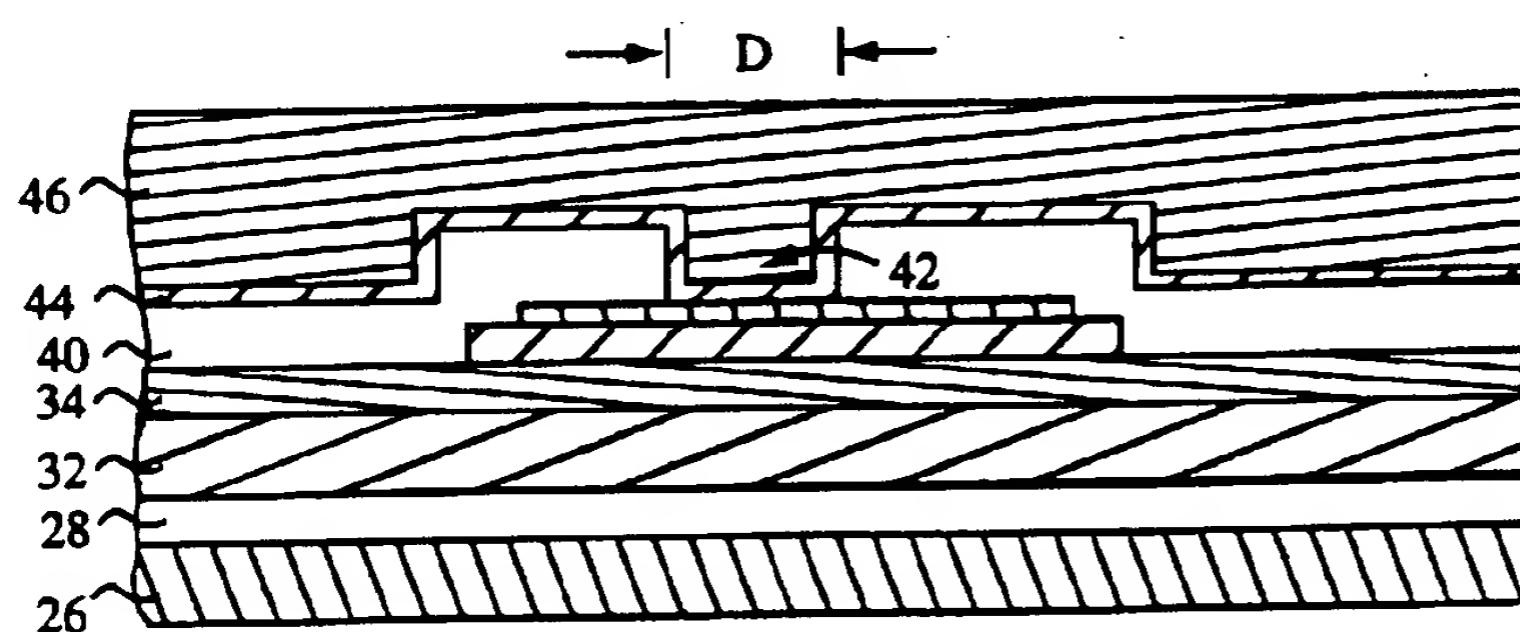


FIG. 4

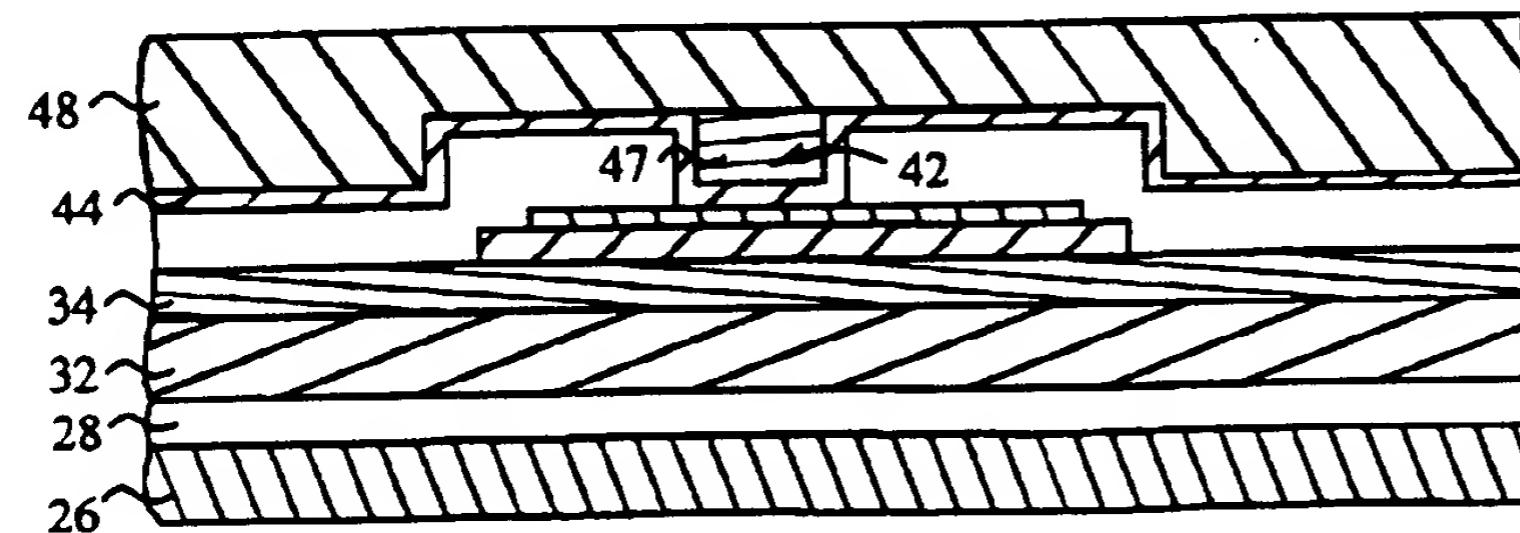


FIG. 5

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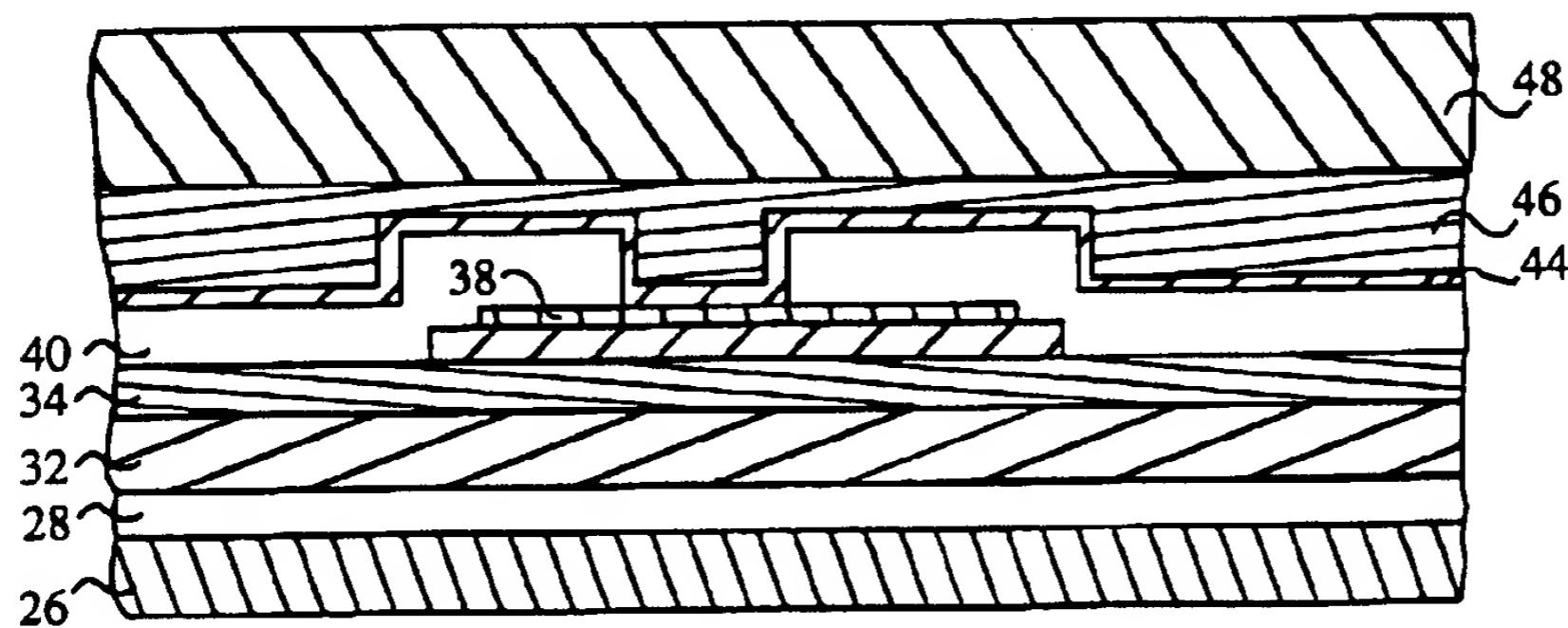


FIG. 6

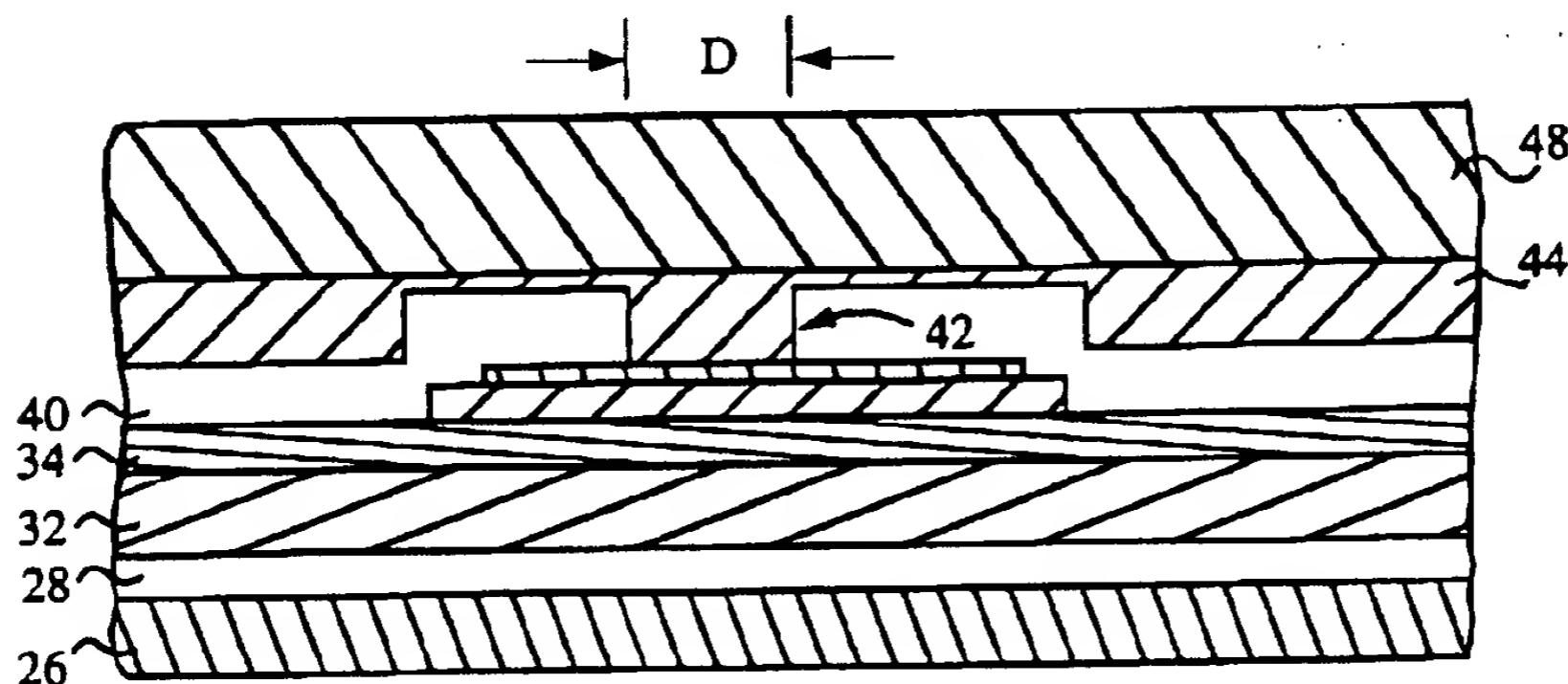


FIG. 7

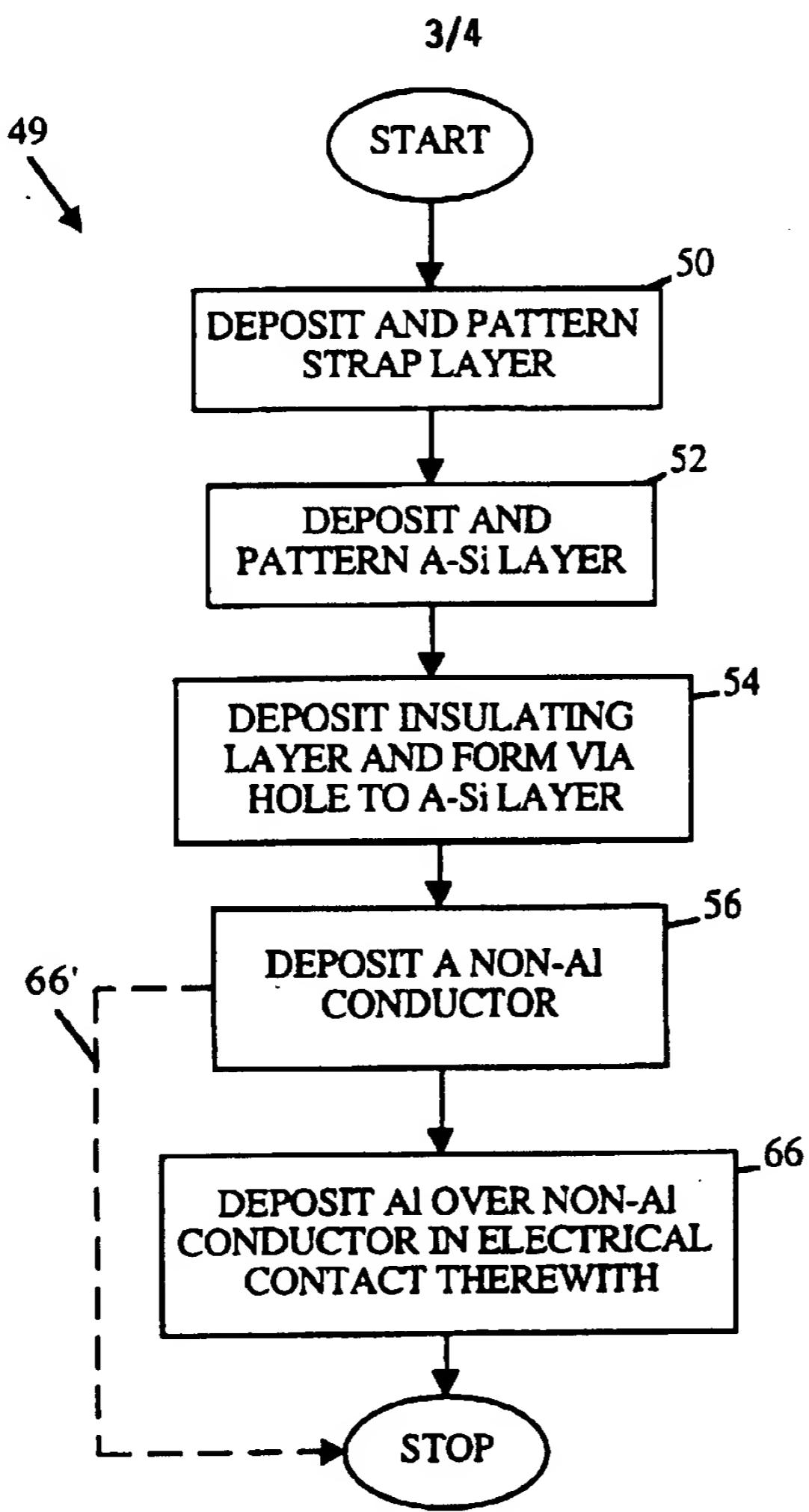


FIG. 8

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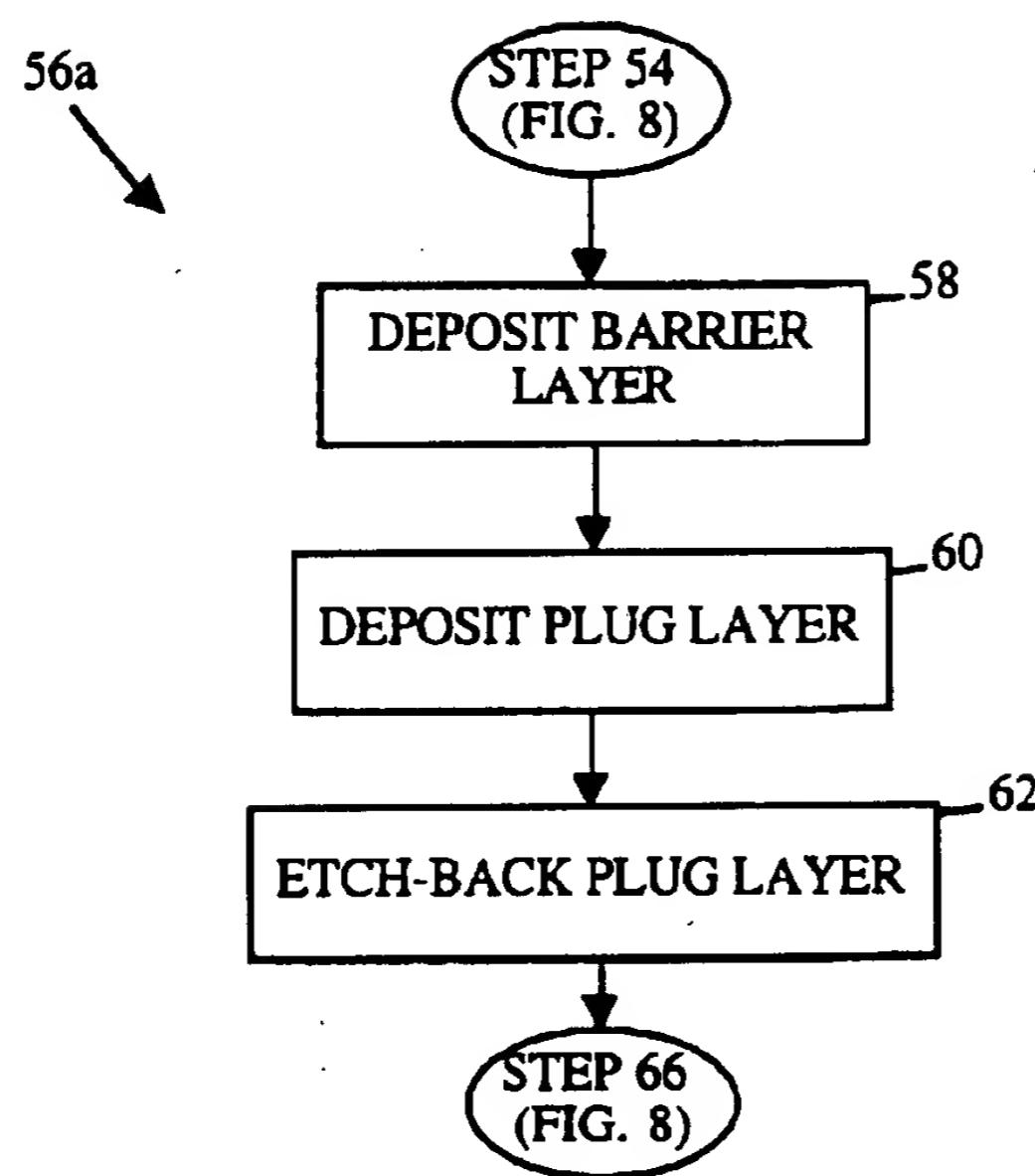


FIG. 9a

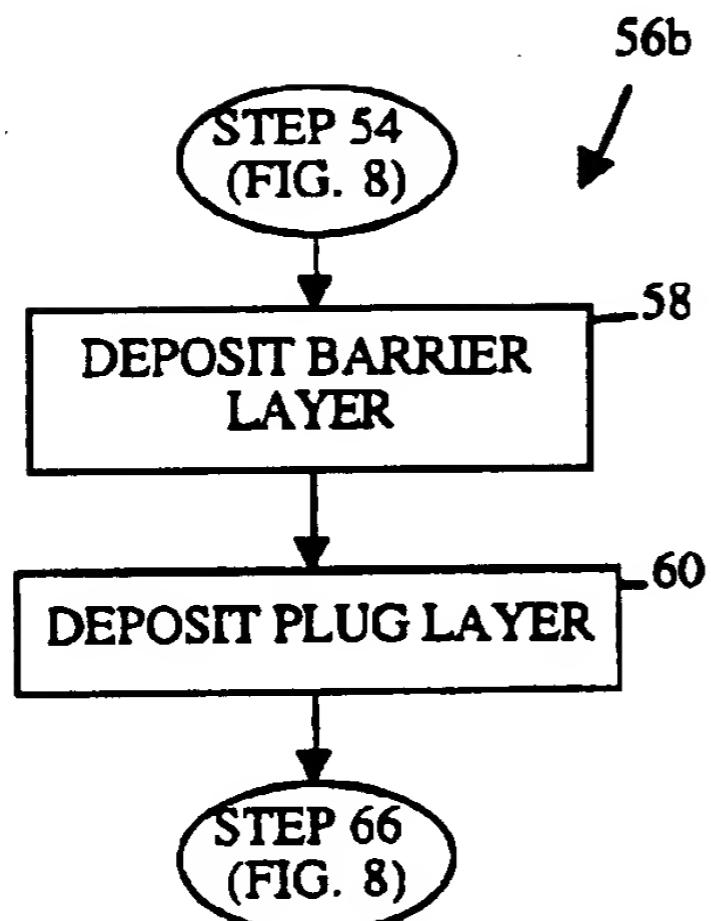


FIG. 9b

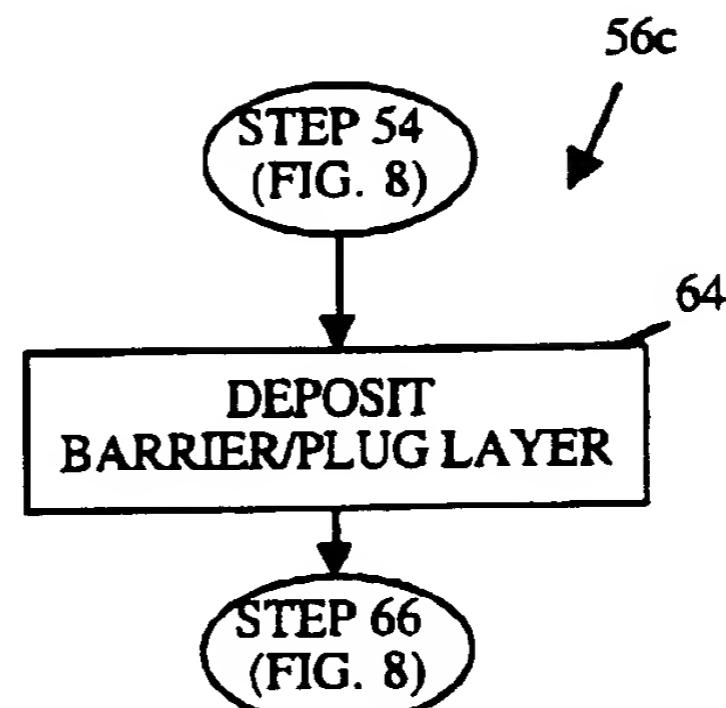


FIG. 9c

INTERNATIONAL SEARCH REPORT

International Application No
PCT/US 95/08795

A. CLASSIFICATION OF SUBJECT MATTER
IPC 6 H01L23/525

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 6 H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	PATENT ABSTRACTS OF JAPAN vol. 017 no. 398 (E-1403), 26 July 1993 & JP,A,05 074947 (FUJITSU LTD) 26 March 1993, see abstract; figures 2,5 ---	1-4, 20-23
A	WO,A,92 20109 (CROSSPOINT SOLUTIONS INC) 12 November 1992 see the whole document ---	1,3-5,8, 11,12, 20, 22-27, 30,31
A	WO,A,93 05514 (VLSI TECHNOLOGY INC) 18 March 1993 see the whole document ---	1,20

Further documents are listed in the continuation of box C.

Patent family members are listed in annex.

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- 'T' later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
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- 'Y' document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
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Date of the actual completion of the international search

31 October 1995

Date of mailing of the international search report

06.11.95

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Fax (- 31-70) 340-3016

Authorized officer

Zeisler, P

INTERNATIONAL SEARCH REPORT

Int. Application No
PCT/US 95/08795

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
P,A	WO,A,95 11524 (VLSI TECHNOLOGY INC) 27 April 1995 see the whole document -----	1,20

INTERNATIONAL SEARCH REPORT

Information on patent family members

International Application No

PCT/US 95/08795

Patent document cited in search report	Publication date	Patent family member(s)		Publication date
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		JP-T-	6511352	15-12-94
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WO-A-9305514	18-03-93	US-A-	5328865	12-07-94
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WO-A-9511524	27-04-95	US-A-	5427979	27-06-95
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